Applicant: FLETCHER, Thomas D
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IN THE CLAIMS:

Please amend the claims to read as follows:

1. (Withdrawn) An apparatus comprising a look-ahead carry adder circuit having a plurality of stages that are grouped into a plurality of carry generation blocks, wherein the size of one of the carry generation blocks is three stages.

2. (Withdrawn) The apparatus of claim 1, wherein other carry generation blocks in the adder circuit are of a size that is a whole number multiple of three stages.

3. (Withdrawn) The apparatus of claim 1, wherein the look-ahead carry adder circuit has a plurality of group propagate gates which each provide a group propagate signal for three stages.

4. (Withdrawn) The apparatus of claim 3, wherein the look-ahead carry adder circuit has a plurality of group generate gates which each provide a group generate signal for three stages.

5. (Withdrawn) The apparatus of claim 1, wherein the look-ahead carry adder has only one critical path.

6. (Withdrawn) The apparatus of claim 5, wherein the look-ahead carry adder circuit has carry generate gates and carry propagate gates that are buffered from the critical path to minimize the load on gates in the critical path.

7. (Withdrawn) The apparatus of claim 1, wherein the look-ahead carry adder circuit includes a plurality of tapered transistor stacks.

8. (Withdrawn) The apparatus of claim 1, wherein the look-ahead carry adder circuit includes at least one gate with a propagate input, a generate input, and only two transistor stacks.

9. (Withdrawn) The apparatus of claim 1, wherein the look-ahead carry adder circuit contains a NAND tree to generate intermediate XOR values.

10. (Previously Presented) A method of adding two multi-bit addends, the method comprising:

receiving two multi-bit addends;

determining a propagate value and a corresponding generate value for each bit of the addends;

determining a carry-out value for each propagate value based at least in part on the propagate value and corresponding generate value, wherein the carry-out values are determined by a plurality of carry generation blocks, and wherein one of the carry generation blocks determines exactly three of the carry-out values; and

determining a sum value for each carry-out value based at least in part of the carry-out value.

11. (Original) The method of claim 10, wherein another of the carry generation blocks determines exactly six of the carry-out values.

12. (Previously Presented) The method of claim 10, wherein the method further comprises determining an intermediate XOR value for each of said propagate values based on the propagate value and corresponding generate value, wherein sum values are based at least in part on the intermediate XOR values, and wherein intermediate XOR values are determined without using an XOR gate.

13. (Original) The method of claim 10, wherein there is a single critical path through the plurality of carry generation blocks.

14. (Original) The method of claim 13, wherein gates in the critical path have tapered transistor stacks.

15. (Original) The method of claim 10, wherein determining one or more of the carry-out values includes combining a propagate value, a generate value, and a carry-in value in a gate that has only two transistor stacks.

16. (Original) The method of claim 10, wherein determining every third carry-out value includes determining a group propagate value and a group generate value.

17. (Original) A look-ahead carry adder circuit, comprising:

inputs to receive two multi-bit addends;

a plurality of blocks each of which is connected to one input bit of both of the multi-bit addends, wherein each block has a propagate output and a generate output;

a plurality of carry generation blocks each having inputs connected to two or more of said propagate outputs and two or more of said generate outputs, wherein one of the carry generation blocks is connected to exactly three of the propagate

outputs and three of the generate outputs, and wherein each of the carry generation blocks has a plurality of carry outputs; and

a plurality of final blocks each of which is connected to one of said carry outputs and each having a sum output.

18. (Original) The look-ahead carry adder circuit of claim 17, wherein another of the carry generation blocks is connected to exactly six of the propagate outputs and six of the generate outputs.

19. (Original) The look-ahead carry adder circuit of claim 17, wherein there is one critical path through the look-ahead carry adder circuit.

20. (Original) The look-ahead carry adder circuit of claim 19, wherein the critical path includes an AND-OR-INVERT gate having an output connected to an input of an INVERT-AND-OR gate.

21. (Original) The look-ahead carry adder circuit of claim 20, wherein the AND-OR-INVERT gate has only two transistor stacks.

22. (Original) The look-ahead carry adder circuit of claim 19, wherein inputs and outputs of gates on the critical path are buffered to reduce the load on the critical path.

23. (Original) The look-ahead carry adder circuit of claim 17, wherein the circuit contains a plurality of tapered transistor stacks.

24. (Original) The look-ahead carry adder circuit of claim 17, wherein some of the carry generation blocks have a plurality of NAND gates that have a pair of inputs that are connected to one of the propagate outputs and one of the generate outputs through one or more buffers, and wherein each of the NAND gates is connected to an XOR output of a carry generation block through a buffer.

25. (Original) The look-ahead carry adder circuit of claim 17, wherein the circuit has a plurality of gates to provide a group generate value and a plurality of gates to provide a group propagate value, and wherein group generate gates are arranged in clusters having a size that is a multiple of three.

26. (Withdrawn) An apparatus comprising a look-ahead carry adder circuit having a plurality of stages that are grouped into a plurality of carry generation blocks, wherein

one of the carry generation blocks is of a size that is a whole number multiple of three stages.

27. (Withdrawn) The apparatus of claim 26, wherein the look-ahead carry adder circuit has only one critical path.

28. (Withdrawn) The apparatus of claim 27, wherein the look-ahead carry adder circuit has carry generate gates and carry propagate gates that are buffered from the critical path to minimize the load on gates in the critical path.

29. (Withdrawn) The apparatus of claim 26, wherein the look-ahead carry adder circuit includes a plurality of tapered transistor stacks.

30. (Withdrawn) The apparatus of claim 26, wherein the look-ahead carry adder circuit includes at least one gate with a propagate input, a generate input, and only two transistor stacks.

31. (Withdrawn) The apparatus of claim 26, wherein the look-ahead carry adder circuit contains a NAND tree to generate intermediate XOR values.

32. (Currently Amended) A method of adding two multi-bit addends, the method comprising:

receiving two multi-bit addends;

determining a propagate value and a corresponding generate value for each bit of the addends;

determining a carry-out value for each propagate value based at least in part on the propagate value and corresponding generate value, wherein the carry-out values

are determined by a plurality of carry generation blocks that include a plurality of tapered transistor stacks wherein in each stack, a transistor at a bottom of each stack is larger than a transistor at a top of each stack; and

determining a sum value for each carry-out value based at least on part of the carry-out value.

33. (Previously Presented) The method of claim 32, wherein the method further comprises determining an intermediate XOR value for each of said propagate values based on the propagate value and corresponding generate value, wherein sum values are based at least in part on the intermediate XOR values, and wherein intermediate XOR values are determined without using an XOR gate.

34. (Previously Presented) The method of claim 32, wherein there is a single critical path through the plurality of carry generation blocks.

35. (Previously Presented) The method of claim 34, wherein gates in the critical path have tapered transistor stacks.

36. (Previously Presented) The method of claim 32, wherein determining one or more of the carry-out values includes combining a propagate value, a generate value, and a carry-in value in a gate that has only two transistor stacks.

37. (Currently Amended) A look-ahead carry adder circuit, comprising:

inputs to receive two multi-bit addends;

a plurality of blocks each of which is connected to one input bit of both of the multi-bit addends, wherein each block has a propagate output and a generate output;

a plurality of carry generation blocks each having inputs connected to two or more of said propagate outputs and two or more of said generate outputs, wherein each of the carry generation blocks has a plurality of carry outputs, and wherein there is one critical path through the plurality of carry generation blocks wherein inputs and outputs of gates on the critical path are buffered to reduce the load on the critical path; and

a plurality of final blocks each of which is connected to one of said carry outputs and each having a sum output.

38. (Previously Presented) The look-ahead carry adder circuit of claim 37, wherein the critical path includes an AND-OR-INVERT gate having an output connected to an input of an INVERT-AND-OR gate.

39. (Previously Presented) The look-ahead carry adder circuit of claim 38, wherein the AND-OR-INVERT gate has only two transistor stacks.

40. (Cancelled)

41. (Previously Presented) The look-ahead carry adder circuit of claim 37, wherein the circuit contains a plurality of tapered transistor stacks.

42. (Previously Presented) The look-ahead carry adder circuit of claim 37, wherein some of the carry generation blocks have a plurality of NAND gates that have a pair of inputs that are connected to one of the propagate outputs and one of the generate outputs through one or more buffers, and wherein each of the NAND gates is connected to an XOR output of a carry generation block through a buffer.